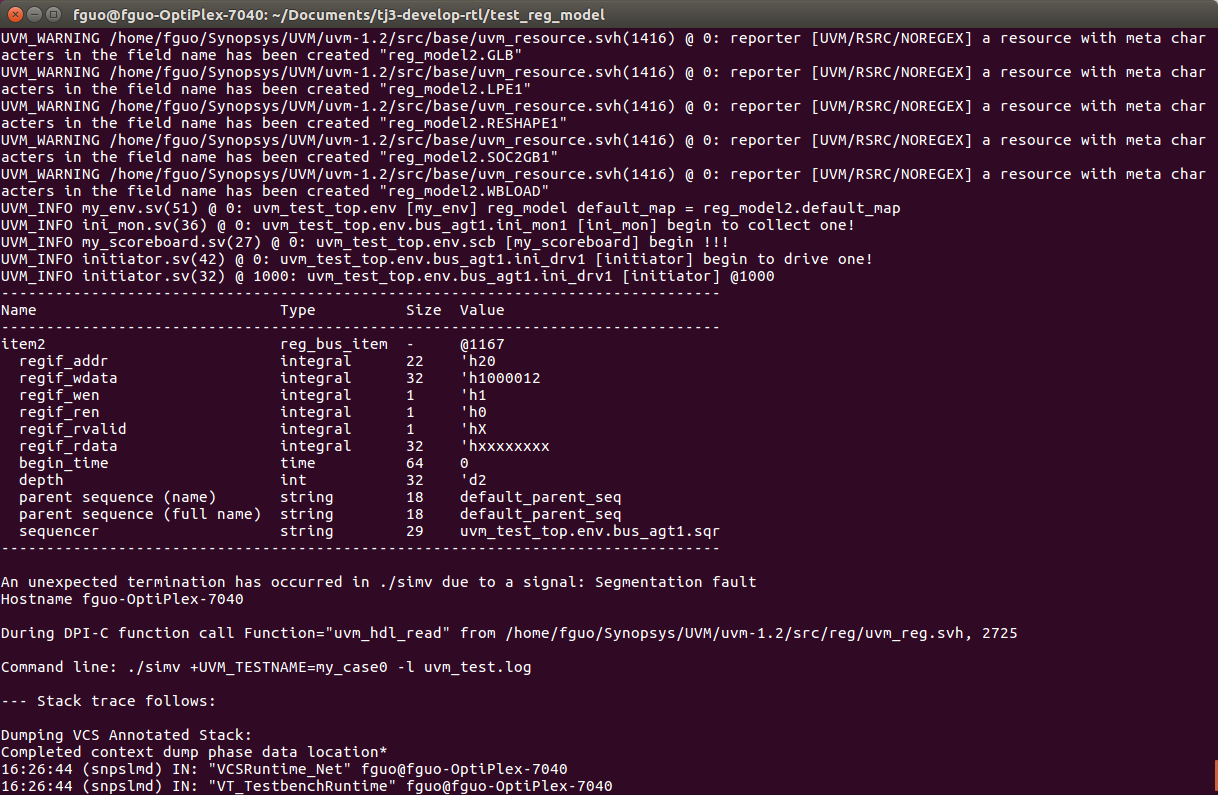
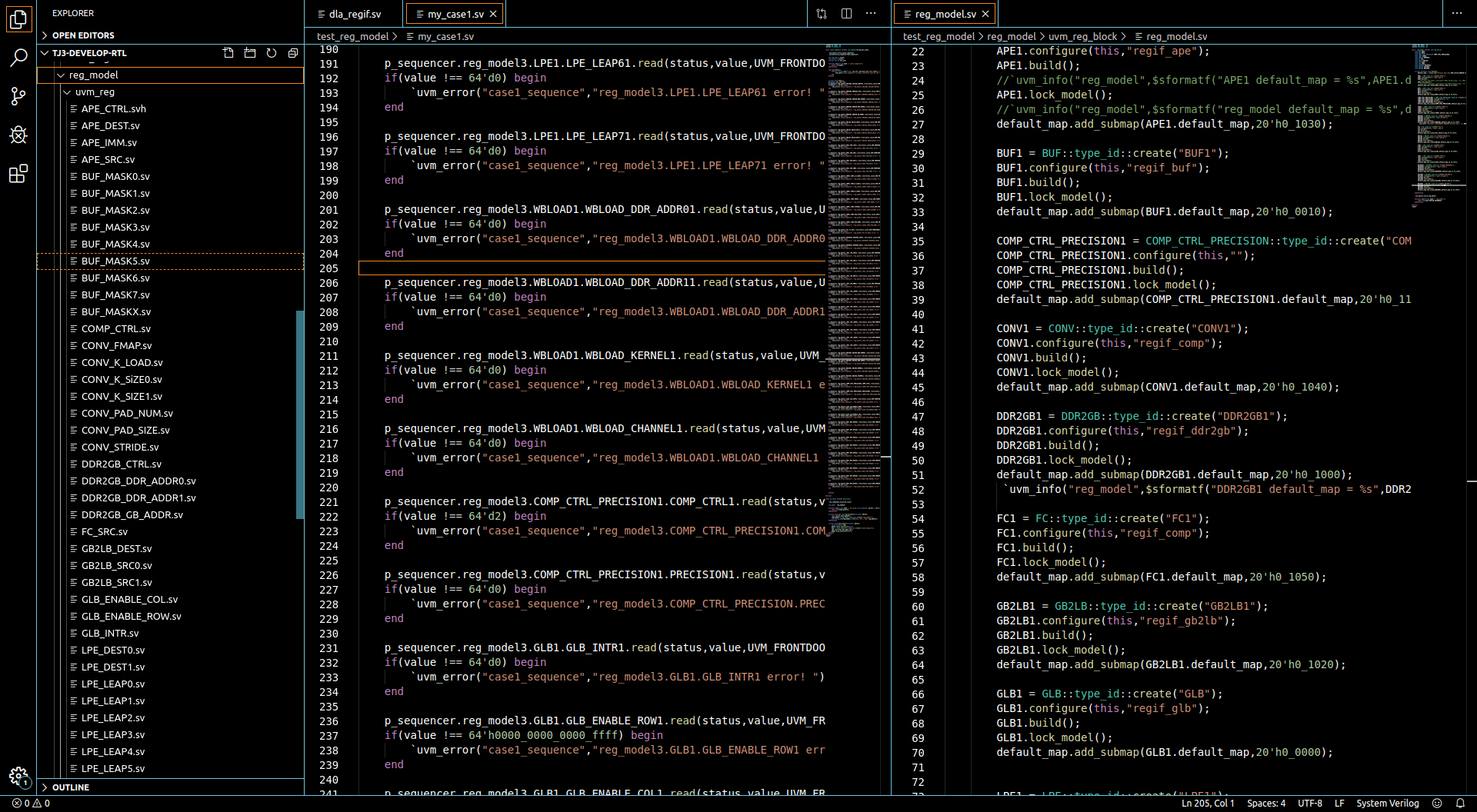
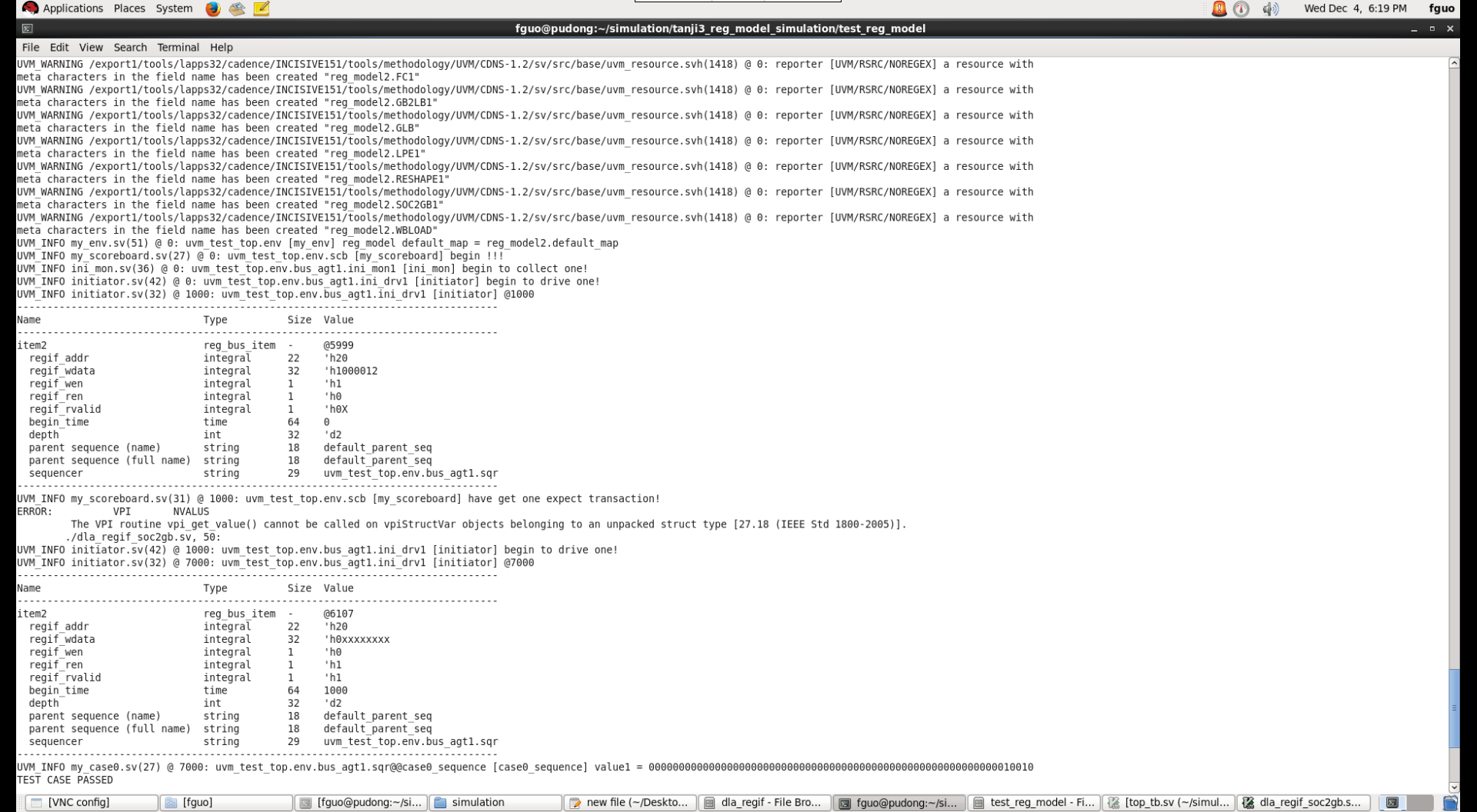
DONE:

1. complete roughly the construction of register model and partially verification of registers.





TO DO:

1. prepare to verify the computing component.